

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENT

Support for the amendments to the claims can be found in the drawings as originally filed, for example, in FIGS. 7 and 8, and in the specification as originally filed, for example, on page 18, line 6 through page 19, line 19. As such, no new matter has been introduced.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-15 under 35 U.S.C. §102(b) as being anticipated by Demos (U.S. Patent No. 5,988,863) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 1, 2, 5, 11 and 13-15 under 35 U.S.C. §102(e) as being anticipated by Chiang et al. (U.S. Patent No. 6,553,072; hereafter Chiang) has been obviated by appropriate amendment and should be withdrawn.

In contrast to Demos or Chiang, the presently claimed invention (claim 1) provides an apparatus comprising (a) a decoder circuit configured to receive an encoded video signal at a first input and to present a decoded video signal at a first output and (b) a scaler circuit configured (a) to receive the decoded video

signal at a second input and a user input signal at a third input and (b) to present (i) a first video output signal having a first resolution at a second output and (ii) a second video output signal having a second resolution at a third output, where the first video output signal and the second video output signal are generated in response to the decoded video signal and the user input signal. Claims 13 and 14 include similar limitations. Neither Demos nor Chiang appear to disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

Specifically Demos does not disclose or suggest a scaler circuit configured (a) to receive the decoded video signal at a second input and a user input signal at a third input and (b) to present (i) a first video output signal having a first resolution at a second output and (ii) a second video output signal having a second resolution at a third output, where the first video output signal and the second video output signal are generated in response to the decoded video signal and the user input signal, as presently claimed. In particular, FIG. 10 of Demos (cited by the Office on page 2 of the Office Action as corresponding to the apparatus of presently pending claim 1) shows four decoders 100, 102, 104 and 106 (see column 15, line 37 through column 16, ,line 11 of Demos). Decoders 100 and 102 each decode part of a single encoded signal

(i.e., Base Layer MPEG-2). Decoders 104 and 106 decode a separate encoded signal (i.e., Enhancement Layer MPEG-2). None of the decoders 100, 102, 104 and 106 appear to receive a user input signal as presently claimed. Therefore, Demos does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over Demos and the rejection should be withdrawn.

Like Demos, Chiang does not appear to disclose or suggest a scaler circuit configured (a) to receive the decoded video signal at a second input and a user input signal at a third input and (b) to present (i) a first video output signal having a first resolution at a second output and (ii) a second video output signal having a second resolution at a third output, where the first video output signal and the second video output signal are generated in response to the decoded video signal and the user input signal, as presently claimed. In particular, assuming, *arguendo*, the HDTV Decompressor 150 of Chiang is similar to the presently claimed decoder circuit and the combination of the 2/3 downampler 170, the multiplexer 175 and the multiplexer 180 of Chiang is similar to the presently claimed scaler circuit (as suggested on page 4 of the Office Action and for which Applicant's representative does not necessarily agree), Chiang fails to disclose or suggest a scaler circuit configured (a) **to receive** the decoded video signal at a

second input and **a user input signal at a third input** and (b) to present (i) a first video output signal having a first resolution at a second output and (ii) a second video output signal having a second resolution at a third output, where **the first video output signal and the second video output signal are generated in response to the decoded video signal AND the user input signal**, as presently claimed. Therefore, Chiang does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over Chiang and the rejection should be withdrawn.

Claims 2-12 and 15-25 depend, directly or indirectly, from either claim 1 or claim 14 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejections should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 16-25 under 35 U.S.C. §103(a) as being unpatentable over Demos (U.S. Patent No. 5,988,863) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claim 25 under 35 U.S.C. §103(a) as being unpatentable over Chiang et al. (U.S. Patent No. 6,553,072; hereafter Chiang) has been obviated by appropriate amendment and should be withdrawn.

Claims 16-25 depend, directly or indirectly, from either claim 1 or claim 14 which, for the reasons presented above in connection with the §102 arguments, are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

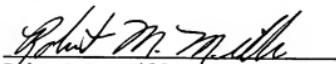
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative between 9:00 a.m. and 5:00 p.m. ET at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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